

Date: December 20, 2017

## EIC Detector R&D Progress Report

**Project ID:** eRD18

**Project Name:** Precision Central Silicon Tracking & Vertexing for the EIC

**Period Reported:** October 1 to December 31, 2017

**Project Leader:** Peter G. Jones

**Contact Person:** Peter G. Jones

### Project Members:

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### Abstract

We propose to develop a detailed concept for a central silicon pixel detector for an Electron-Ion Collider at BNL or JLab exploring the advantages of using HV-CMOS or HR-CMOS MAPS technologies. The sensor development exploits the newly created Birmingham Instrumentation Laboratory for Particle Physics and Applications. An accompanying simulation study seeks to optimise the basic layout, location and sensor/pixel dimensions to find the best achievable momentum resolution and vertex reconstruction resolution. This initial design study will allow future full-detector simulations to explore precision measurements of heavy flavour processes and scattered electrons at high  $Q^2$ .

## 1 Past

### 1.1 *What was planned for this period?*

Our proposed programme of work for FY18 was divided into two work packages: WP1 on sensor development and WP2 on detector layout investigations.

The aim of WP1 is to demonstrate the advantages of Depleted Monolithic Active Pixel Sensors (DMAPS) over standard (non-depleted) MAPS. The key difference between the two is that in a depleted sensor, charge collection is achieved primarily through drift rather than by diffusion. This has the potential to generate larger signals, faster charge collection and reduced charge sharing between pixels, leading to better signal-to-noise, improved time resolution and improved spatial resolution. The plan for this period was to begin work characterising two investigator chips from the TowerJazz (TJ) foundry, fabricated in both standard (MAPS) and modified (DMAPS) processes. These chips have a variety of pixel matrices (8 x 8 pixels) containing pixels ranging in size from 20 x 20  $\mu\text{m}^2$  to 50 x 50  $\mu\text{m}^2$ , each with a single collection electrode. The same pixel matrices are available on both chips allowing a

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direct comparison of signal rise time and amplitude for identical pixels fabricated in the two processes.

The aim of WP2 is to optimise the detector layout of the central barrel through simulation studies of charmed hadron decays and high  $Q^2$  scattered electrons. This work is being carried out in collaboration with eRD16 who focus primarily on the forward tracking regions. In our report and presentation to the Committee in July, we showed the results of initial studies on momentum resolution and impact parameter resolution for electrons in a standalone silicon tracker modelled in EicRoot. This allowed us to compare directly with the results of eRD16, which demonstrated a good level of agreement between EicRoot and eRD16's simplified simulation framework. We also showed the first results of full detector simulations for pions and pixel sizes of  $20 \times 20 \mu\text{m}^2$ ,  $30 \times 30 \mu\text{m}^2$  and  $40 \times 40 \mu\text{m}^2$ . The momentum resolution was shown to be rather insensitive to choice of pixel size at low transverse momentum ( $p_T < 5 \text{ GeV}/c$ ), whereas the impact parameter resolution clearly favours smaller pixels, particularly for the innermost layers. The plan for this period was to focus on charm reconstruction, optimising the number of layers, the resolution of each layer and integration with the forward disks.

## 1.2 What was achieved?

We report here on the progress made on WP1: sensor development. This work has been carried out by Håkan Wennlöf, a new PhD student, who will spend the next 3-4 years working on EIC detector development and related physics. For the purposes of this report, we focus on a comparison of  $28 \times 28 \mu\text{m}^2$  pixels fabricated in the TJ standard<sup>†</sup> and modified processes. Each pixel has a single  $2 \times 2 \mu\text{m}^2$  n-type collection electrode separated by  $3 \mu\text{m}$  from a surrounding deep p-well. The collection electrode is connected to an input transistor and a reset transistor. The output signal is proportional to the ionisation charge collected on the input transistor. A substrate voltage of  $V_{\text{sub}} = -6 \text{ V}$  was applied and this is thought to be sufficient to provide full depletion of the sensor volume in the modified process [1].

The sensor chips were exposed to a  $^{55}\text{Fe}$  source. Data were acquired until 1200 hits had been recorded. After removing spurious hits that did not have the expected waveform shape, the resulting signal rise time (10%-90%) and signal amplitude were plotted. Fig. 1 shows the correlation between signal rise time and signal amplitude comparing pixels fabricated in the standard and modified processes. There are 989 accepted hits in the standard process histogram (left panel) and 898 accepted hits in the modified process histogram (right panel). It is immediately clear that there are significantly more large-amplitude signals from the pixel fabricated in the modified process, which is expected due to more complete charge collection by drift. This is confirmed by comparing the pulse height spectra, which are shown in Fig. 2, where the  $K_\alpha$  and  $K_\beta$  peaks of the  $^{55}\text{Fe}$  source are clearly distinguished in the modified process. In fact, there are approximately four times more counts in the  $K_\alpha$  peak in the right panel of Fig. 2.

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<sup>†</sup> The standard process is the one being used for the upgrade of the ALICE Inner Tracking System.

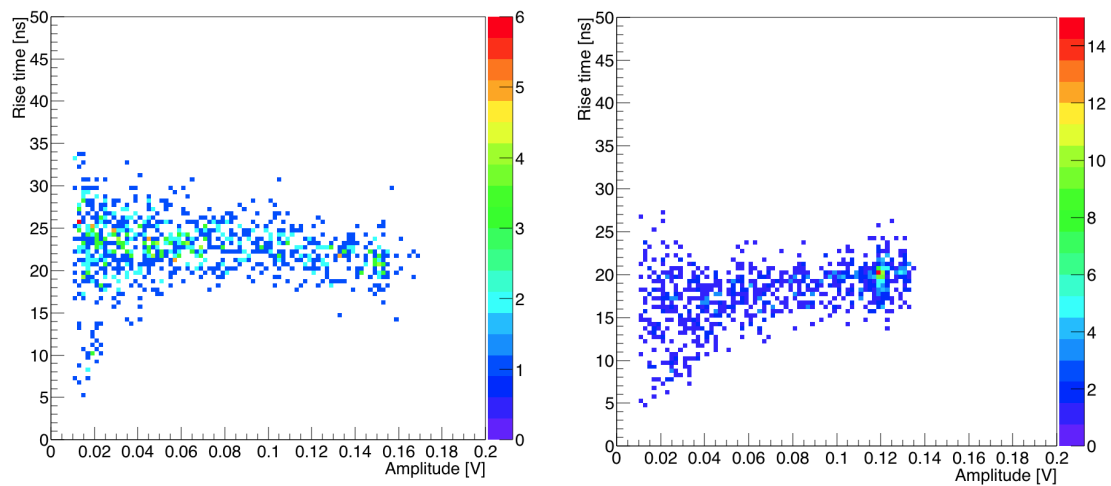


Figure 1. Rise time versus signal amplitude for a  $28 \times 28 \mu\text{m}^2$  pixel fabricated in the TJ standard process (left) and in the modified process (right).

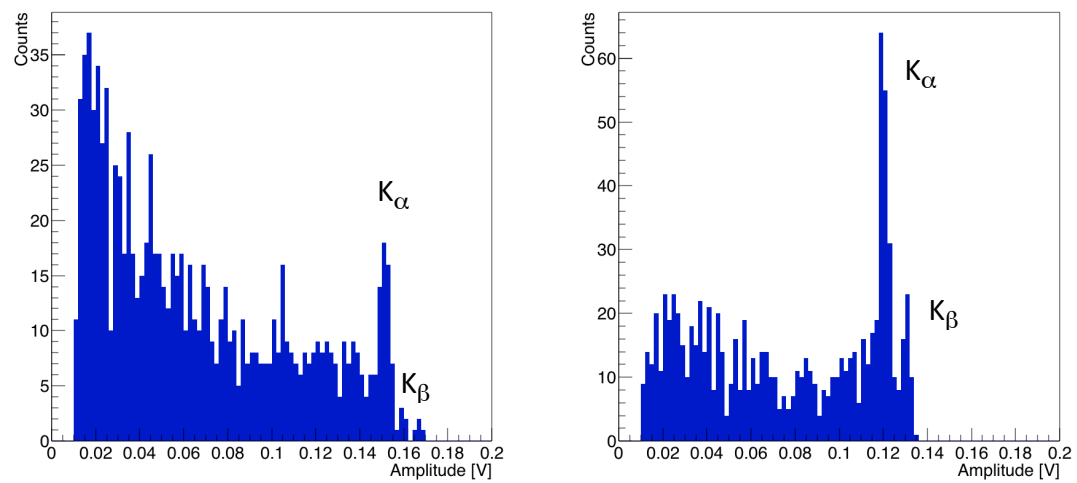


Figure 2. Signal amplitude for a  $28 \times 28 \mu\text{m}^2$  pixel fabricated in the TJ standard process (left) and in the modified process (right).

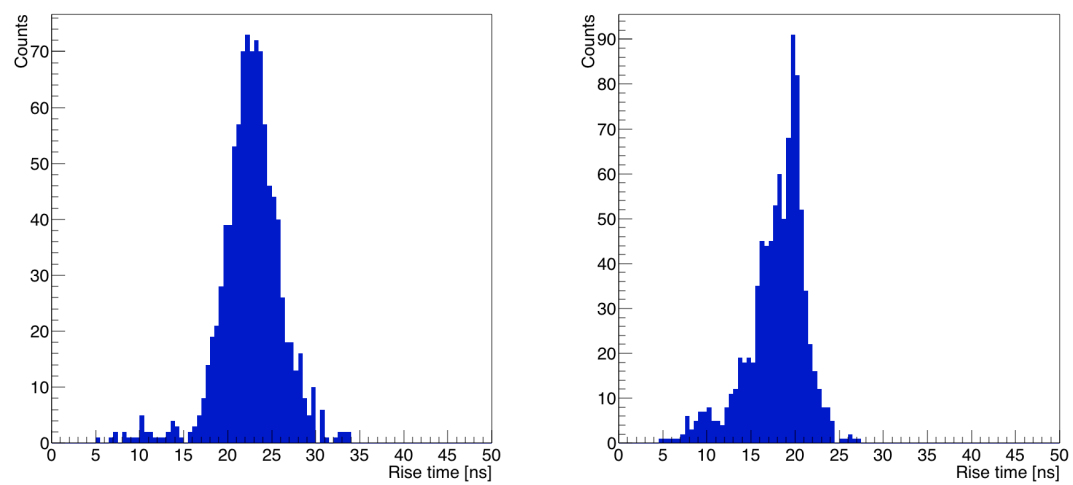


Figure 3. Signal rise time for a  $28 \times 28 \mu\text{m}^2$  pixel fabricated in the TJ standard process (left) and in the modified process (right).

Fig. 3 compares the signal rise time for each pixel. There is a modest improvement for the pixel fabricated in the modified process. The mean rise time in the standard process is  $22.6 \pm 3.6$  ns, whereas in the modified process the mean rise time is  $17.9 \pm 3.4$  ns. Faster rise times are expected in the modified process due to faster charge collection by drift.

These results are broadly in agreement with studies published elsewhere [1]. In comparison with those earlier studies, Fig. 1 seems to indicate a slight dependence of the rise time with the signal amplitude in the modified process, which has not been seen before. This appears to be due to the signal amplifier having a shorter decay time in the test setup at Birmingham. Comparable measurements made with a similar test setup at the University of Glasgow show no dependence. A replacement amplifier will therefore be used for future measurements.

### ***1.3 What was not achieved, why not, and what will be done to correct?***

Our postdoc, Sam Bailey, who was performing the detector layout simulations associated with WP2, left in the summer when our FY17 EIC funds ran out. No further progress has been made on the simulations in this reporting period. However, we are now beginning to return the simulations and expect to give an update to the Committee at the January meeting. Now that the test setup associated with WP1 is up and running and code written to analyse the data, our PhD student will begin to familiarise himself with the EicRoot framework, working from an internal report written by Sam before he left [2].

Our plans for this funding cycle remain unchanged and are still achievable. The specific questions we plan to address are:

- How many layers are needed and at what radii?
- What is the required pixel resolution at each layer?
- What is the optimal length of the barrel layers and what overlap in acceptance with the forward disks is possible/desirable?

These questions will be addressed through simulation of charm decays in the EicRoot framework. In collaboration with eRD16, at the end of the current funding cycle we aim to have defined the detector layout and to have an initial set of specifications for the sensors that may be used in the central barrel tracker and the forward disks.

## **2 Future**

### ***2.1 What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?***

In the next (FY19) funding cycle, further work will be required to fully characterise the TJ investigator chips in the standard and modified processes. We also expect to be in a position to explore other sensor options that will become available

through our involvement in other projects. In summary, we will investigate the following:

- TJ investigator chip in both standard and modified processes, pixel sizes ranging from  $20 \times 20 \mu\text{m}^2$  to  $50 \times 50 \mu\text{m}^2$ , single collection electrode.
- DECAL prototype chip in the TJ standard process (available since November 2017) and test structures in the TJ modified process,  $50 \times 50 \mu\text{m}^2$  pixels, multiple collection electrodes.
- RD50 LFoundry submission, various pixel sizes and functionalities, now not expected until the end of 2018. However, we are currently performing TCAD simulations with two masters project students, which will provide some comparative data for pixels with large and small collection electrodes.

As the Committee is already aware, we are considering the possibility to involve a chip designer at RAL to put some thought into different readout design options. This work would complement the detector layout simulations by starting to look at the readout capabilities of the sensor. A key question that needs to be addressed is the timing capability that can be built into the readout given the pixel size and an estimate of the power consumption for different readout architectures. The aim here is not to fully define the readout, but to explore what is possible and at what cost in terms of power and speed. We will begin to address these questions already in FY18, but expect this to continue into the next funding cycle.

## 2.2 What are critical issues?

Although not necessarily a critical issue, the question of timing capability has not yet been fully addressed. The potential need for a single event, barrel tagger has been considered by the tracking and PID consortium (eRD6) and was discussed briefly at the last meeting. This was foreseen to be a separate layer between the inner silicon barrel and out tracking detector. We would like to consider whether a fast timing silicon layer could perform this function. The outermost layer requires a spatial resolution commensurate with the pointing resolution of the outer tracker. This raises the possibility of a (relatively) low resolution, outer silicon tracking layer with fast timing. To fully address this question requires a calculation of the optimal pixel size from the perspective of particle tracking together with an estimate of the expected occupancy and collision rate, as this will determine the data rate off detector. The input of a chip designer, as mentioned above, will be required to estimate the power requirements of such as detector.

## 3 Manpower

*Include a list of the existing manpower and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located and who supervised their work.*

Prof. Peter Jones (0.05 FTE) – no cost to project

Dr. Laura Gonella (0.1 FTE) – no cost to project

Dr. Sam Bailey (0.5 FTE) – postdoc, funded for 5.5 months from EIC funds

Håkan Wennlöf (1.0 FTE) – PhD student, funded by the University of Birmingham

Prof. Phil Allport and Prof. Paul Newman have had an advisory role and participate in our regular project meetings to monitor progress.

## 4 External Funding

*Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.*

EIC R&D (FY17) funds supported a postdoc for 5.5 months, which enabled us to make a start on the detector layout simulations within the EicRoot software framework.

This project receives the support of a PhD student funded by the University of Birmingham. We have submitted a bid for funds to support some of the R&D elements of this proposal as part of the EU Horizon 2020 NextDIS consortium.

## 5 Publications

*Please provide a list of publications coming out of the R&D effort.*

Not applicable at this stage of the project.

## 6 References

[1] H. Pernegger et al., First tests of a novel radiation hard CMOS process for Depleted Monolithic Active Pixel Sensors, 2017 JINST 12 P06008.

[2] S. Bailey, EIC Tracker Simulations with EicRoot, Internal Report, University of Birmingham, August 10, 2017.